J Mater Sci (2009) 44:545–555
DOI 10.1007/s10853-008-3083-2

# Very long-term aging of 52In–48Sn (at.%) solder joints on Cu-plated stainless steel substrates

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Received: 27 June 2008 / Accepted: 23 October 2008 / Published online: 23 November 2008


**Abstract** Long-term metallurgical aging was studied in thermal switches comprised of 52In–48Sn (at.%) alloy solder plugs contained in Cu-plated stainless steel cylinders. These switches are locking devices designed so that, if overheated, a "fusible" alloy melts and allows the activation of a spring-loaded mechanism. The soldered assemblies studied ranged in age from about 24 to 28 years old at the time of this analysis. A concern has been the buildup of intermetallic compound (IMC) within the solder or at the solder/substrate interface, which could raise the switch operating temperature. In this work, the melting temperature of the aged solder alloy was slightly *lower* (116.3 ± 0.3 °C) than the expected value, 118.4 °C (245 °F), based on differential scanning calorimetry (DSC). The slight decrease in melting temperature range was caused by the diffusion of a small amount of Cu into the solder during processing and possibly during long-term service. The interfacial IMC layer was primarily $Cu_2In_3Sn$. The IMC thickness agreed with that predicted by growth kinetics determined in a previous study, assuming aging temperatures in the vicinity of room temperature. Differences in the IMC phase chemistries were found between earlier research, which employed bulk Cu substrates, and the present analyses with thin electroplated Cu substrates. Evidence was found for depletion of the thin Cu plating layer over time, as well as incorporation of Fe and Ni from the stainless steel into the IMC layer.

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## Introduction

A thermal switch was designed so that when a solder plug melts, the switch actuates. The switch was constructed with a Cu-plated 15-5 PH stainless steel housing and a 52In–48Sn (at.%) alloy solder "plug." After prolonged storage, it was thought that intermetallic compound (IMC) growth in the solder and at the solder/substrate interface could raise the actuation temperature of the switch. This concern was initially addressed in a previous study of switches designed with only a thin solder layer [1]. The IMC growth kinetics were determined using Sn–In/Cu diffusion couples over a temperature range of 70–110 °C [1, 2]. In [2], the sample geometry was a piston and cylinder, both made of bulk Cu, with a thin solder layer in between. Quantitative measurements were made for layer growth of two IMC layers, identified as $Cu_2(In,Sn)$ and $Cu_2In_3Sn$. A subsequent investigation was performed by Vianco and coworkers on Cu samples hot dipped in 50In–50Sn and subjected to aging at 70, 85, and 100 °C for up to 200 days [3]. They also found two IMC layers, but with slightly different compositions. The extreme variations observed in the layer thicknesses precluded a quantitative assessment of layer growth kinetics.

More recent work was performed by Sommadossi et al., also on bulk Cu substrates [4]. The solder alloy was 52In–48Sn (at.%) and they investigated temperatures from 180 to 400 °C using a diffusion soldering process (note: the solder was in the liquid state). They described the layer growth kinetics and morphology of the IMC layers, including $Cu_2(In,Sn)$ and $Cu_2In_3Sn$, both of which were also described by Romig and coworkers [2]. Another recent investigation was that of Chuang and coworkers, who studied soldering and IMC growth kinetics in the 51In–49Sn/Cu system at 60–110 °C [5]. Two IMC phases were

found which were reported to be related to $\varepsilon$-$Cu_3(In,Sn)$ and $\eta$-$Cu_6(In,Sn)_5$. Solid-state growth exhibited activation energies of 29 and 186 kJ/mol for the two phases, respectively. Finally, Kim and Jung recently studied the solid-state IMC growth kinetics for 52In–48Sn/Cu at 70–100 °C [6]. They identified the IMC phases as $Cu(In,Sn)_2$ and $Cu_6(In,Sn)_5$ and gave an activation energy of 95 kJ/mol for the combined IMC layers and 98 kJ/mol for the individual $Cu_6(In,Sn)_5$ layer.

As shown above, most recent literature has been concerned with IMC growth on bulk Cu substrates and at fairly high temperatures associated with soldering or accelerated solid-state aging. Different IMC phases were identified by different researchers and there are also different IMC layer growth kinetics. The differences in layer compositions could indicate a metastability of the phases as a function of the aging temperatures. No investigations of IMC layer growth were found for Sn–In solder in contact with *Cu-plated* stainless steel. Also, there has been no report on long-term aging of this solder/substrate system at low temperatures, e.g., near ambient. For eutectic Sn–In solder, room temperature represents a homologous temperature of approximately 0.75. Thus, it is possible that significant diffusion can take place at room temperature over long time periods. The present investigation was undertaken to determine the melting behavior, IMC growth characteristics, and solder microstructure for Sn–In/Cu–plated stainless steel assemblies that experienced long-term aging. The samples were in the field for approximately 24–28 years prior to this analysis. It was established that the components were stored at, or very near, room temperature throughout their service lifetimes. The observed IMC phases were analyzed by electron probe microanalysis (EPMA) and the results discussed with reference to the binary In–Sn and ternary Cu-In–Sn phase diagrams.

## Experimental procedure

Differential scanning calorimetry (DSC) was performed on a Perkin–Elmer DSC-7. The DSC was calibrated by a two-point calibration process using pure indium and pure zinc with melting points of 156.6 and 419.5 °C, respectively. To determine the melting behavior of the 52In–48Sn (at.%) solder, the DSC experiments were run at a heating rate of 10 °C/min, from 25 to 300 °C, and then cooled back to 25 °C at the same rate. For strict comparisons of DSC experiments with published phase diagrams, slower temperature scan rates should be used. However, for the relative comparisons between In–Sn solder and aged thermal switch samples in this study, it is believed that the 10 °C/min scan rate is acceptable, especially for the on-heating transformation which is less sensitive to scan rate than the undercooling effect during solidification.

The peak onset temperatures were determined by Pyris version 1.1 DSC software. With this software, the onset temperature is chosen by constructing a tangent line from the inflection point in the endotherm. The intersection of this tangent line with the baseline tangent determines the onset temperature. To prepare for the DSC tests, the solder plug/housing assemblies were cross-sectioned longitudinally, slightly off-center. The larger piece of solder was used for metallographic analysis. A smaller piece of solder was removed from its housing with a razor blade and used for DSC. The mass of each DSC sample was approximately 5 mg. It was not possible to include the thin layer of IMC material at the solder/substrate interface to determine its melting temperature. For comparison to the aged thermal switch solder, pure 52In–48Sn solder obtained from the manufacturer was also analyzed by DSC. It should also be noted that traditional DSC experiments often employ multiple melting/solidification cycles to completely homogenize the material to accurately identify the melting and solidification temperatures. In this study, however, the initial melting behavior of the (nonhomogenous) solder plug was of interest.

To analyze the microstructure of the solder and IMC layer, samples were mounted in cold-setting epoxy. Grinding was performed with 600 grit SiC paper using water as the lubricant. Polishing was done with 15 and 6 μm diamond polishing media with nylon cloth. These steps were followed by a 1-μm diamond polish on a napped cloth. Final polishing was performed either manually with 0.02-μm $SiO_2$ on a napless cloth or on a vibratory polisher with low nap cloth using 0.02-μm $SiO_2$ for 30 min. The samples were cross-sectioned in the longitudinal direction, as discussed above, and polished to the center of the solder plug. Although this procedure is less desirable than a transverse cross section for measuring layer thickness, the final polished cross-sectional plane was determined to be sufficiently near the center of the cylindrical plug, thereby minimizing the resulting error in the layer thickness measurements. The IMC layer thickness was measured using optical microscopy and quantitative image analysis (QIA) on a Clemex Vision PE system. Two hundred IMC thickness measurements were performed on each image obtained at 200 times magnification. A total of nine (9) images (approximately 1,800 total thickness measurements), taken along the length of the IMC layer, were used to gather the thickness statistics from each sample. The number of images allowed for analysis of greater than 2.2 mm of the solder/substrate interface on each sample. In addition, due to the distinct color of the Cu-plated layer, color-based QIA was used to aid in distinguishing the IMC layer from the other materials.

The estimated error in IMC thickness measurement with the image analysis technique was approximately ±1 to 1.5 μm. The experimental error comes from three main sources. First, at 200× the pixel size was 0.24 μm per pixel. Assuming that the placement of the measurement line is off by one pixel on each side of the IMC layer, the estimated pixel resolution error is approximately ±0.48 μm. Second, sample preparation artifacts can affect the IMC layer thickness measurements. For example, a dark line was present in the images between the IMC layer and the solder due to differences in the polishing behavior of the hard IMC layer and the soft solder. The thickness of this dark line was determined to be about 2 pixels. Therefore, it is believed that placement of measurement lines at the IMC/solder interface varies by about ±1 pixel (±0.24 μm) due to this artifact. Finally, threshold errors are possible, i.e., error during the delineation/selection of the IMC layer. The IMC layer was selected by first thresholding the Cu electroplated layer based on color. The interface between the electroplated Cu and the IMC layer was defined very precisely with this technique. The dark line at the interface between the IMC and the solder was used to define this edge of the IMC layer. The errors in this procedure were minimal and were already accounted for in the pixel resolution and sample preparation artifacts discussed above. All of these sources of experimental error were small in comparison to the actual thickness variation of the undulating (scalloped) IMC layer. This thickness variation was on the order of ±7.5 μm about the average thickness.

To determine the composition of the solder and IMC phases, EPMA was performed with wavelength dispersive spectroscopy (WDS) on a JEOL 8600 at 15 kV operating voltage and 30 nA probe current. Multiple EPMA traces were made on two samples, beginning in the stainless steel substrate, passing through the Cu-plating layer if present, and ending in the bulk solder alloy, using 1 μm steps. The microstructures of the IMC layers and the solder were documented by scanning electron microscopy (SEM) in secondary and backscatter (BSE) modes using a Zeiss Supra 55VP SEM.

## Results and discussion

### Melting behavior of aged Sn–In thermal switches

The DSC technique was used to determine the melting behavior of the In–Sn solder, i.e., the solidus and liquidus of the alloy. This approach differs from previous experiments in which the thermal switches were slowly heated and the operating temperature of the device was used as a measure of the "melting point" (internal results, Sandia National Laboratory, Albuquerque, NM, USA). The melting temperature estimated in that manner may not correspond directly with DSC experiments. For example, when heating an entire component there may be a temperature lag of a few degrees between the furnace temperature and the internal solder plug temperature, even for slow heating rate experiments. In addition, the temperature at which the device operates may not correspond to the *onset* of melting (the solidus), but rather to the overall melting of the bulk solder.

Figure 1 shows portions of the DSC heating curves from four In–Sn samples obtained from the thermal switches. The onset of the endothermic melting peak was taken as the solidus by convention. The average solidus temperature was 116.3 ± 0.3 °C (241.3 ± 0.5 °F). As shown in Fig. 1, the four experiments displayed nearly identical melting characteristics. The peak maxima occurred at 117.7 ± 0.3 °C (244 ± 0.5 °F). The steep slope of the melting peak is typical of a eutectic or near-eutectic alloy. The solder samples begin melting at lower temperatures when compared to the previous work mentioned above. Some previous work on thermal switches suggested a possibility that the melting range of the solder plug was increasing with age, presumably due to IMC formation, but the recent results for even older thermal switches do not support that trend. Confirmation of the effect of Cu impurity was obtained by running DSC experiments on pure 52In–48Sn material obtained from the solder manufacturer. During heating, the melting onset temperature of the pure solder was 118.4 °C (also shown in Fig. 1), which agrees with the manufacturer's stated melting point of 118 °C.

According to the In–Sn phase diagram in Fig. 2, the eutectic point occurs at 120 °C and corresponds to the 52In–48Sn alloy. Note that the eutectic temperature has

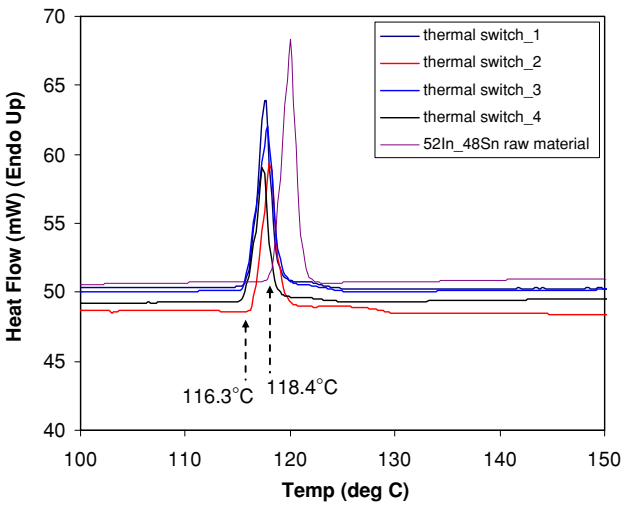



**Fig. 1** Portions of heating curves of four DSC samples of Sn–In alloy from aged thermal switches and as-received 52In–48Sn solder

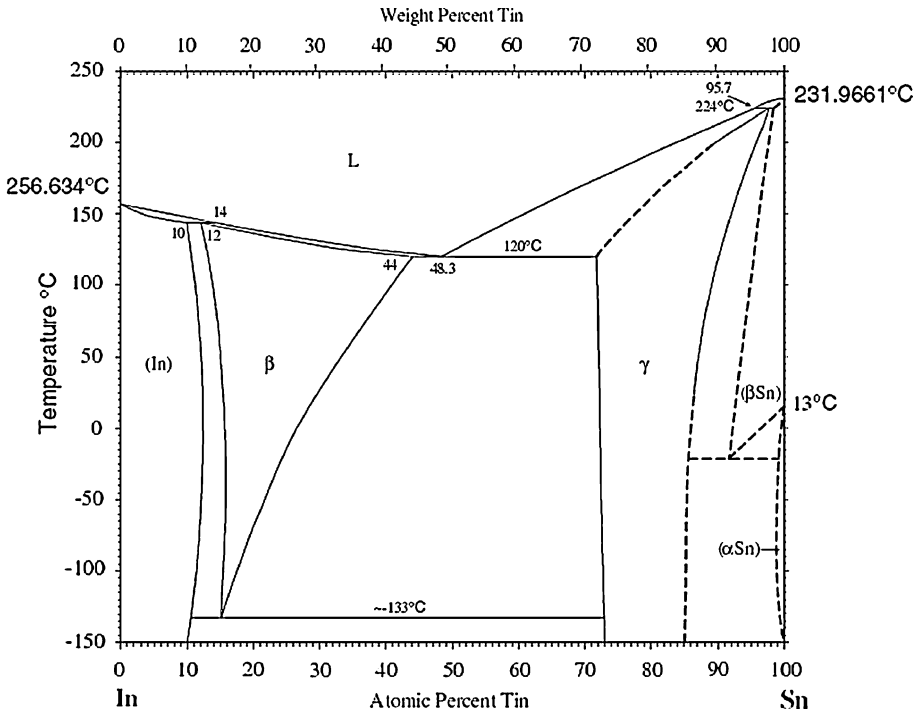



**Fig. 2** In–Sn binary phase diagram [7]

been reported between 118 and 120 °C by various researchers [6–10]. The onset of melting of 116 °C found for thermal switch material in this study is lower than either value, albeit with a 10 °C/min scan rate which may be too high for strict comparison to phase diagrams Nevertheless, while a difference of 2° is small, it is sufficiently larger than the expected experimental scatter in peak position. This was shown by performing multiple DSC runs with binary 52In–48Sn solder. Two samples were analyzed with four runs performed on each sample. These eight analyses, when combined with the 52In–48Sn scan shown in Fig. 1, gave the following average onset temperature and standard deviation: 118.18 ± 0.11 °C (average and standard deviation of nine DSC experiments). This estimate of run-to-run variation of 0.11 °C is much lower than the 2 °C difference between the thermal switch samples and the binary In–Sn solder shown in Fig. 1. The likely cause for the decrease in temperature of melting onset is a small amount of Cu that diffused into the solder during soldering and/or during long-term aging. Evidence for small amounts of Cu within the solder plug was found by SEM and EPMA, both of which will be shown later. Figure 3 displays a portion of the ternary Sn–In–Cu liquidus projection. The binary Sn–In eutectic point (e1) is shown along the right side of the diagram. As small amounts of Cu are added, the liquidus of the ternary alloy decreases toward the ternary eutectic point (E1). According to the research by Liu et al., the ternary eutectic melting point is 111.2 °C at only 0.71 wt% Cu [8]. Therefore, small additions of Cu to a eutectic In–Sn alloy will reduce the alloy melting range, which explains the

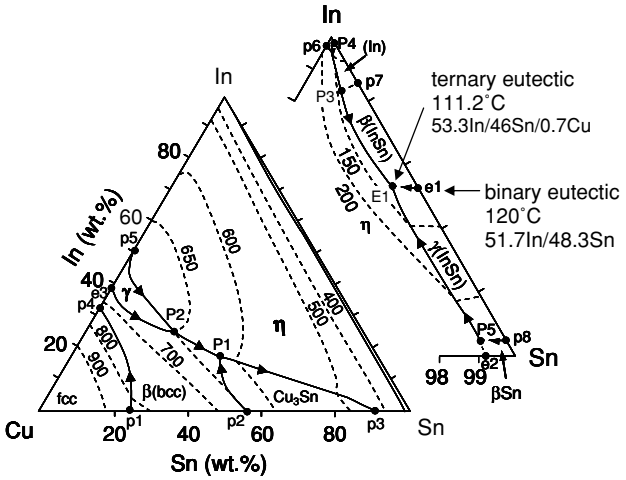



**Fig. 3** Ternary liquidus projection, from [8], showing the Sn–In binary eutectic and Sn–In-Cu ternary eutectic points

lower melting temperatures found in Fig. 1. The broad shoulders on the right side of the DSC peaks are also an indication that the alloy is slightly off-eutectic [11]. The shoulders are formed due to continuous melting of off-eutectic (primary phase) material between the solidus and liquidus of the alloy. The 52In–48Sn raw material (unaged), on the other hand, does not show a shoulder on the trailing edge of the DSC peak. This behavior is more indicative of a eutectic alloy which transforms at a single temperature. It is noted, however, that trace amounts of primary phase and/or a narrow temperature separation between the solidus and liquidus could result in small

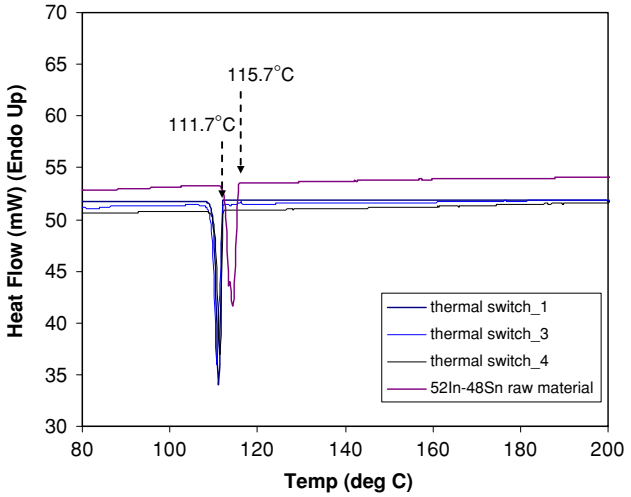



**Fig. 4** Portions of the cooling curves of DSC samples showing the solidification peaks from aged thermal switches and as-received 52In–48Sn solder

shoulders that are "buried" underneath and not discernable within a larger DSC peak.

The cooling segments of the DSC curves were also analyzed. Figure 4 shows the cooling curve data from the same DSC experiments shown in Fig. 1. Upon cooling, the alloys re-solidify at a lower temperature compared to their onset of melting on heating, due to the undercooling effect. The solidification temperatures of the aged thermal switch alloys were 111.7 ± 0.3 °C. For the 52In–48Sn raw material, the solidification temperature was found to be 115.7 °C. Thus, approximately 3–5 °C of undercooling is experienced in these DSC experiments for both thermal switch material and for the pure solder material. Notice also that the solidification peaks for the aged thermal switch material are more symmetric (no broad shoulder), after homogenization of Cu in the alloy in the liquid state, suggesting eutectic-like solidification behavior. In summary, the incorporation of a small amount of Cu into the solder caused the samples taken from the thermal switches to display melting properties like those of an off-eutectic ternary Sn–In–Cu alloy and, after liquid homogenization, the alloy behaved more like a ternary eutectic alloy on solidification.

## IMC characterization and layer growth kinetics

Figure 5a shows the cross-sectional microstructure of the Sn–In solder and the IMC layer observed in a thermal switch. The Cu-plated stainless steel substrate is also shown. Two IMC layers are observed—a thin layer adjacent to the Cu plating and a thicker, faceted layer extending into the solder field. In Fig. 5b, the QIA processed image is shown with the lines used for automated measurement of IMC thickness. Note that the distinct color of the Cu plating was used to separate the IMC layer from the Cu-plated substrate during image processing. In this study, a total of nine photomicrographs were obtained from each sample, resulting in approximately 1,800 thickness measurements along the lengths of the IMC layers.

Figure 6a and b shows the field of view with the thickest observed IMC layer. A large IMC crystal was found growing into the solder field in this region. It is likely that this crystal is a product of the solder solidification process and not strictly a result of the interdiffusion process during long-term aging. However, no morphological distinction was made between these two types of IMC. This was done to avoid judgment of intermediate cases where small primary crystals at the interface might look similar to the typical undulations of the IMC interfacial layer. Therefore, any IMC in contact with the interface was included in the thickness measurements. Only two obvious cases of large crystals, such as the one shown in Fig. 6a and b, were found. Thus, the low number of thickness measurements associated with them were not enough to appreciably alter the IMC thickness results (since about 1,800 thickness measurements were performed on each sample). At the thickest IMC location shown in Fig. 6a, the total IMC layer thickness across the sample was 132 μm; that is, 78 μm at this side of the joint and 54 μm at the joint on the opposite

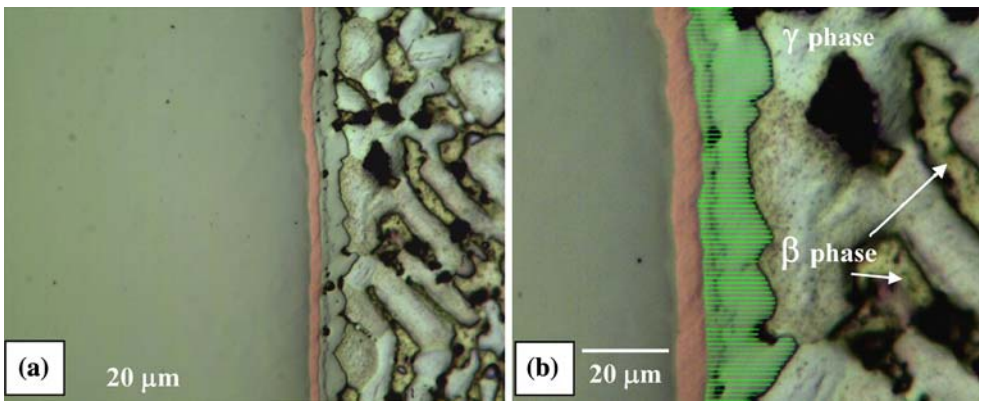



**Fig. 5** **a** Color optical photomicrograph of (*left to right*) stainless steel substrate, Cu plating layer, IMC layer(s), and Sn–In solder and **b** IMC layers highlighted with individual thickness measurement lines

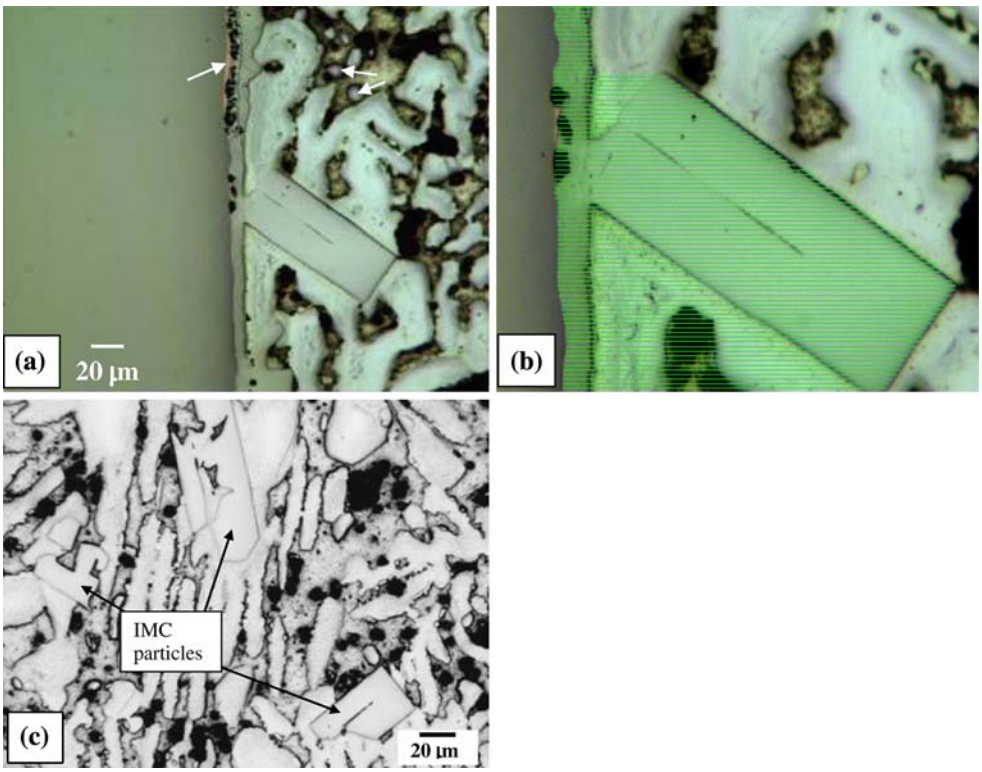



**Fig. 6** **a** The field of view showing the largest observed IMC crystal growing into the solder field (sample 2) (Also shown in (**a**) are small particles within the solder alloy (arrows in solder). These were identified as particles of metallographic polishing compound (SiC or diamond) that were embedded in the soft solder, especially in the In-rich phase, during sample preparation), as well as depletion of residual Cu layer. **b** Higher magnification image with IMC layer thickness measurement lines. **c** IMC particles within the solder microstructure

side of the solder plug cylinder. Other large IMC crystals were found in the thermal switch units, within the solder field (Fig. 6c), and the composition of these crystals will be discussed later. In contrast, the *average* IMC layer thickness measured in all units was $34 \pm 8$ μm, or approximately 17 μm on average on each side of the solder plug cross sections. This value represents only a small fraction of the total thermal switch diameter. While a 17-μm thick IMC layer seems appreciable when compared to other studies of IMC growth [3], it represents only a small fraction of the total thermal switch volume. Therefore, the interface IMC layer would not affect the overall melting temperature range of the solder plug.

The blocky IMC phase that formed within the solder field (Fig. 6c) has the same composition as the large interfacial crystal, with a significant amount of Cu (see EPMA results discussed later). The formation of these relatively high-Cu crystals during solidification indicates that the solder contains Cu at the solubility limits of the individual solder phases. As described earlier, the presence of these IMC particles with considerable Cu is supporting evidence that Cu contamination caused the melting point depression observed in the DSC experiments.

Several other morphological features were noteworthy in Fig. 6. In Fig 6a, only a thin residual Cu plating layer is observed (arrow). In fact, the Cu layer was completely missing along appreciable lengths of the interface. In general, regions that displayed thin Cu layers also exhibited Kirkendall voids near the interface. These voids, which are also visible in Fig. 6a, are caused by different solid-state diffusion rates of the various elements across the interface, resulting in uneven mass transport of atoms between the Cu layer and the In–Sn–(Cu) solder. The amount of Kirkendall voiding varied from sample to sample. When voiding is particularly severe along the interface, they are able to link up into a continuous path that could cause a loss of hermeticity or mechanical bonding at the interface. However, the interfacial voiding did not appear to be of such an extent that compromised these properties. The reason(s) for the differences in residual Cu thickness and Kirkendall porosity observed among the thermal switch samples is not fully understood, but it could be related to variations in the original plating thickness during manufacturing.

It was assumed that the thermal switch storage temperatures were 23 °C throughout their service life. It was possible to quantitatively predict the IMC layer growth

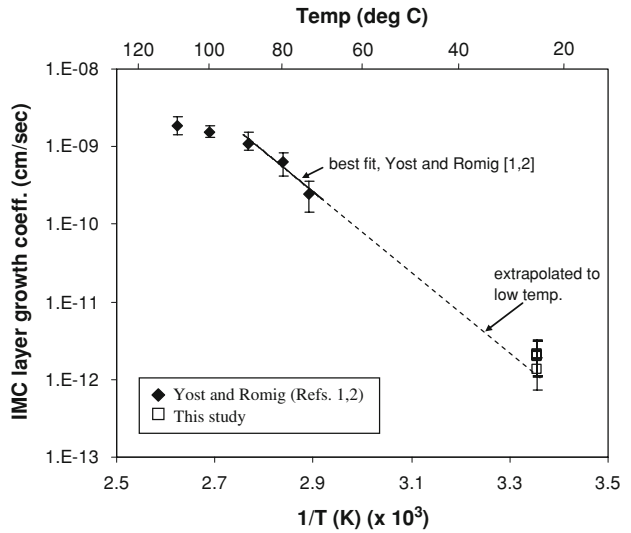



**Fig. 7** IMC layer growth coefficient (log scale) versus reciprocal temperature. The trend obtained by Yost and Romig [2] was extrapolated to low temperatures

kinetics based on the previous work of Yost and Romig, which was performed at higher temperatures and shorter times. Figure 7 shows a plot of the IMC layer thickness versus reciprocal temperature plot from [2], along with the data points obtained in the present study. Yost and Romig found two different kinetic regimes. At higher temperatures (100 and 110 °C), they interpreted the layer growth kinetics to be controlled mainly by bulk (volume) diffusion having a parabolic time dependence. At lower temperatures of 70–90 °C, they concluded that an interfacial reaction was the rate-controlling process by the linear time dependence.

During linear IMC growth, the layer growth may be described by the equation:

$$\xi = \xi_o + st$$

where $\xi$ is the total layer thickness at any time, $\xi_o$ is the initial layer thickness (immediately after soldering), $t$ is time (s), and $s$ is the layer growth coefficient. To use this kinetic equation, the initial IMC layer thickness must be known. For the present study, the initial layer thickness was assumed to be 1.5 μm. This is similar to the approximate initial layer thickness in a previous study of Sn–In IMC growth [3]. In contrast, in the work by Yost and Romig, their initial layer thickness was 3.4 μm. However, they used a two-stage solder dip process of 3–15 s at 250 °C followed by 40–360 s at 180 °C. It was deemed that this two stage process, with relatively long times and high temperatures, was responsible for the thicker initial IMC layer. In any case, the present kinetic calculations were repeated with different initial thickness values ranging from 1 to 3 μm and the changes in the position of data points in Fig. 7 were insignificant.

Yost and Romig were able to fit a line to the kinetic results at the three lower temperatures (70, 80, and 90 °C) with a slope yielding an activation energy of $Q =$ 18,600 cal/mole (77.8 kJ/mol). This line is extrapolated down to room temperature in Fig. 7. The extrapolated best-fit line lies close to the thermal switch data points of the present study, aged at room temperature over long service lifetimes. The error bars shown with the recent data points are due to actual variations in the layer thicknesses along the length of the interface (see Figs. 5 and 6) and are not associated with errors in measurement technique (image resolution, sampling errors, etc.). Typically, agreement of kinetic data within an order of magnitude is judged to be acceptable. With this in mind, the results shown in Fig. 7 are of interest in two respects. First, the agreement between the 70–90 °C data of Yost and Romig and the long-term/low-temperature results of the present work shows the usefulness of accelerated aging experiments to predict component lifetimes near room temperature, for which short-term experimental results are difficult to interpret. Second, the change in kinetics shown by Yost and Romig at higher temperatures suggests, however, that caution must be exercised when extrapolating very high temperature accelerated aging results to low temperatures. There may be a mechanism change between the two temperature regimes.

There were other experimental differences between previous studies and the present work. The primary difference was that the Yost and Romig study used bulk Cu as one end member of the diffusion couples. In the present investigation, the substrate is stainless steel with a *thin Cu plating layer*. Full depletion of the Cu layer would remove the source of Cu required for Cu–In–Sn IMC layer growth. Evidence for depletion of the Cu plating layer was already shown in Fig. 6. It may be hypothesized that this depletion of Cu could present a "limiting mechanism" to slow or stop further IMC layer growth. However, this hypothesis has yet to be experimentally verified. Also, the effects of elements from the stainless steel substrate diffusing into the IMC layer and/or the solder were not considered in the kinetic analysis presented above. These effects will be discussed further below.

## Electron probe microanalysis

Three EPMA traces were performed on cross sections of each of two units to further identify the IMC layers at the Cu-plated stainless steel/solder interface. Figure 8 shows a typical profile (sample 1). This particular sample showed a residual Cu plating layer with thickness of approximately 5 μm. Figure 9 displays an EPMA trace, from sample 2, which runs through a region with no residual Cu plating layer. In Figs. 8 and 9, the stainless steel composition, on

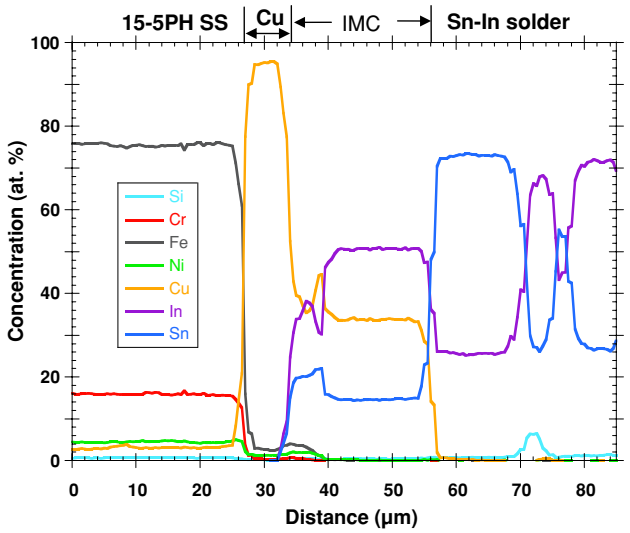
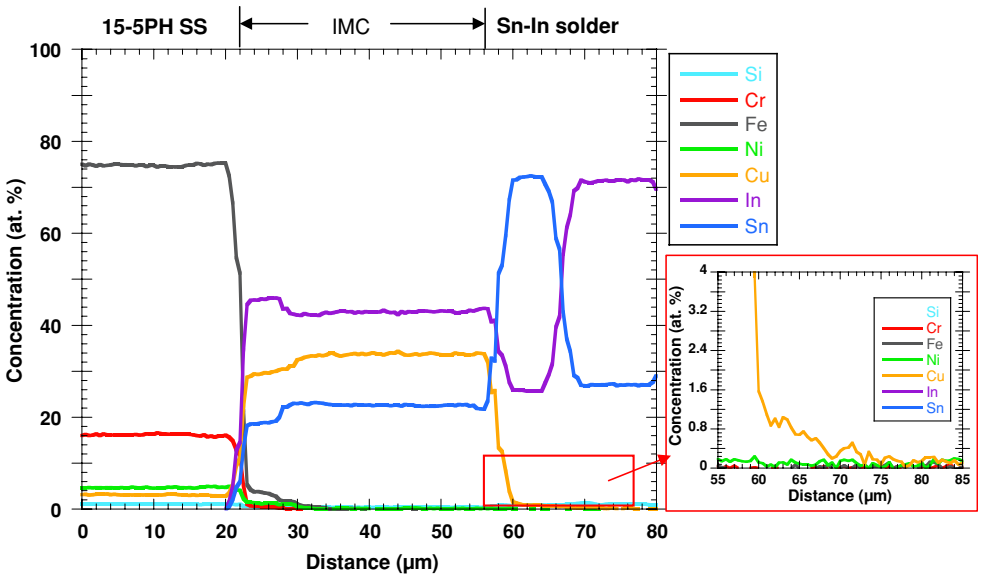



**Fig. 8** EPMA trace through the stainless steel, residual Cu plating, IMC layer, and into the Sn–In solder of sample 1

the left side of the plots, matches well with alloy 15-5PH. The accuracy of the EPMA data is shown by the correct values of the minor elements of Cu and Si, at approximately 3 and 0.5 at.%, respectively. On the right side of Fig. 9, the compositions of the two phases of the bulk solder are shown. The In-rich phase is $\beta$ which has 72 at.% In and 28 at.% Sn. The Sn-rich phase is $\gamma$ having 73 at.% Sn and 27 at.% In. These compositions are consistent with the $\beta$ and $\gamma$ equilibrium phase boundaries at room temperature, as shown in Fig. 2 [7]. These two phases comprise the eutectic microstructure of this solder, as shown on the right side of Figs. 5 and 6. The solder adjacent to the IMC layer is made up almost exclusively of the Sn-rich $\gamma$ phase (Figs. 5, 6, 8, and 9), a result of Sn rejection during IMC layer growth [1, 2]. The low, intermittent Si signal in the bulk solder is due to embedded particles of metallographic polishing compound.

In Fig. 8, the IMC layer thickness is approximately 18 μm and the layer displays two regions with slightly different compositions, which correspond to the two different IMC morphologies observed in Fig. 5. The composition of the thicker IMC layer (average and standard deviation of 27 EPMA points) is 33.7 ± 0.55 at.% Cu, 50.7 ± 0.22 at.% In, and 14.8 ± 0.62 at.% Sn (in wt%: 22.0Cu–59.7In–18.0Sn). Based on the ternary Cu–In–Sn phase diagram, determined by Liu and coworkers [8], this IMC phase was identified as $Cu_2In_3Sn$. Similar IMC layer chemistries were found in previous studies by Romig et al. and Vianco et al., as shown in Fig. 10. With compositions in wt%, Fig. 10 shows the Cu–In–Sn isothermal section at 110 °C, which is the lowest available temperature in the literature for this ternary system. As shown in Fig. 10, the other EPMA traces on the two analyzed samples had slightly different compositional ranges, yet were close to the $Cu_2In_3Sn$ phase. The reason for the somewhat different EPMA results from those traces was not determined. The $Cu_2In_3Sn$ IMC was the major (thicker) layer in this work as well as in the study by Romig and coworkers [2]. However, in the work by Vianco et al., an IMC layer with a composition close to $Cu_2In_3Sn$ was found to be the thinner layer in their samples [3]. The differences in the relative layer thicknesses in these various investigations could be due to experimental differences. For example, Vianco et al. used Cu samples hot-dipped into molten 50In/50Sn solder and aged at 70–100 °C. On the other hand, the IMC phases in the present study grew from

**Fig. 9** EPMA trace through the stainless steel, IMC layer, and into the solder of sample 2. Inset shows slight diffusion of Cu into the solder field



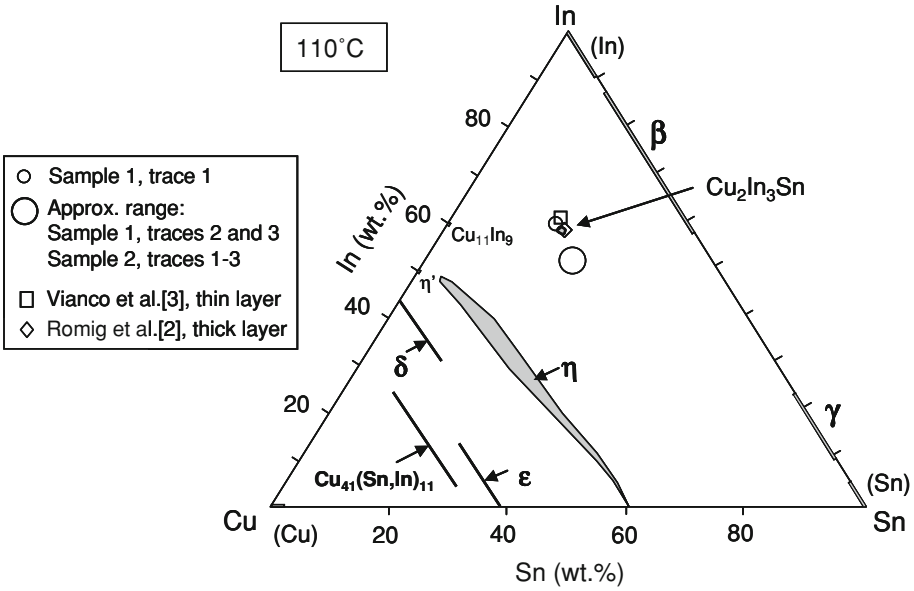



**Fig. 10** Ternary Cu–In–Sn isothermal section at 110 °C (calculated and determined experimentally, [8]). The measured compositions of ternary IMCs are shown from this study (room temp. aging) and other studies by Romig et al. [2] and Vianco et al. [3] (70–110 °C aging)

a finite "source" of Cu via the plated layer, thereby reflecting the metastable nature of phases that grow at interfaces.

Referring to Fig. 8, it is interesting that elements from the stainless steel, including Fe and Ni, have diffused into the Cu layer and built up slightly at the Cu/IMC interface. It is unlikely that this diffusion occurred during the soldering step, due to its short duration. Instead, the diffusion occurred primarily during long-term solid-state aging at low temperature. The presence of these elements could explain the compositional differences between the thin IMC layer (next to the Cu layer) and the main $Cu_2In_3Sn$ layer. The proposed scenario is that Fe and Ni diffuse into the Cu plating layer and then the Cu layer reacts to form IMC during long-term diffusion. The residual Fe and Ni are rejected from the IMC layer, depositing near the IMC/Cu interface. Thus, the two IMC layer compositions (Figs. 5 and 8) represent "consumption" of the Cu plating layer and, concurrently, IMC growth into the solder field. If the trace amounts of Fe and Ni are assumed to substitute for Sn, In, and Cu in their relative proportions in the EPMA data, an adjusted "ternary" composition for this IMC layer can also be plotted on the phase diagram (Fig. 11). When compared to $Cu_2In_3Sn$, it appears that the thinner IMC layer contains higher Cu, lower In, and lower Sn. The more Cu-rich IMC layers from the previous studies [2, 3] are also shown. For sample 1, although the IMC composition is near the $\eta$ phase, it was not close enough to confirm this equilibrium phase. The thin IMC adjacent to the Cu layer is either simply a nonequilibrium composition of the $\eta$ phase,

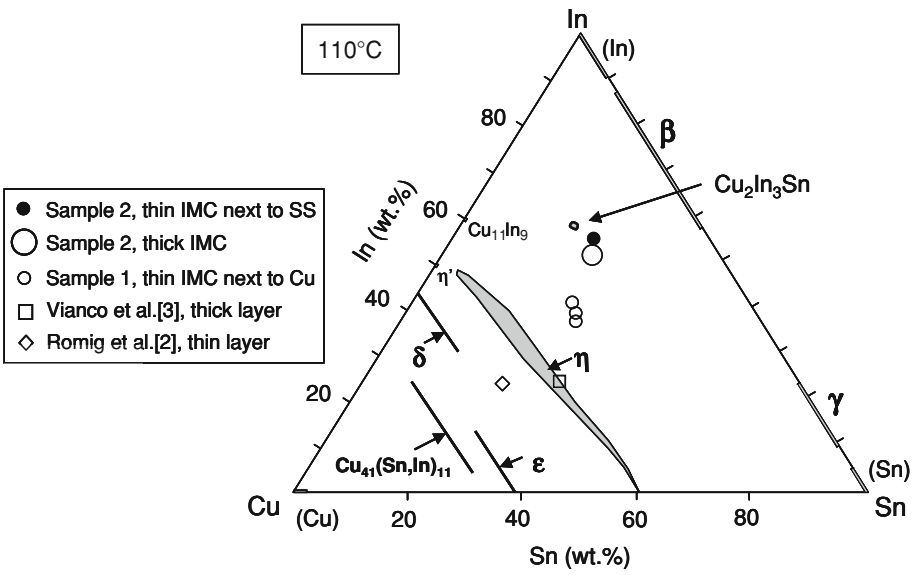



**Fig. 11** Ternary Cu–In–Sn isothermal section at 110 °C, adapted from [7]. Measured compositions of thin IMC layers are shown along with Cu-rich IMCs from Romig et al. [2] and Vianco et al. [3]

or it is a different nonequilibrium phase. Nonequilibrium, metastable phases are not uncommon for thin IMC layers. It should be noted that the two previous studies, discussed above, also displayed a second IMC layer adjacent to the Cu side of the diffusion couples. The second layer in the study by Romig et al. was identified as $\delta$ phase, $Cu_2(In,Sn)$. In the work by Vianco et al., the second layer was the thicker layer which also had a more Cu-rich composition of $Cu_{26}Sn_{13}In_8$. Again, the differences among these investigations, in particular the presence of elements from the stainless steel in the current study, preclude further generalization about the more Cu-rich IMC layer.

The EPMA scan from sample 2 (Fig. 9) traversed through a region with no residual Cu plating layer. The total IMC layer thickness in this location was approximately 35 μm. Based on the average and standard deviation of 46 EPMA points, the major layer had a composition of 33.7 ± 0.31 at.% Cu, 43.0 ± 0.26 at.% In, and 22.6 ± 0.28 at.% Sn (in wt%: 21.9Cu–50.4In–27.4Sn). This approximate composition was also plotted on the ternary diagram in Fig. 10 (in wt%). This layer, again, appears close to the $Cu_2In_3Sn$ phase, but with a slightly lower In content.

The inset in Fig. 9 shows a close-up view of the IMC/solder interface showing evidence for the diffusion of Cu into the solder field. The approximate depth of Cu diffusion is about 15 μm, after which the Cu concentration drops to the resolution limit of the EPMA system. Although the Cu penetration depth is fairly shallow, the evidence does suggest some solid-state Cu diffusion took place into the solder over the long aging times of the thermal switch. This Cu diffusion, combined with the Cu dissolved during the soldering operation discussed previously, provided the sources of Cu in the solder that were responsible for the melting point depression revealed by the DSC analysis.

The thinner IMC layer adjacent to the stainless steel appears to have a different, more In-rich, composition than that shown in Fig. 8 for sample 1. The second IMC layer in Fig. 9 also appears to show lower relative amounts of Sn and Cu when compared to the main IMC layer. The thin IMC layer also contains small amounts of Fe and Ni originating from the stainless steel. It appears that, as the Cu plating layer becomes fully depleted, there is an increase in the In concentration in the IMC layer that subsequently grew adjacent to the stainless steel. This outcome differs from the case shown in Fig. 8, in which a more Cu-rich layer is present adjacent to the Cu plating layer. In sample 2 (Fig. 9), it is possible that the elements from the stainless steel are substituting for Cu, and to some extent Sn, which have lower values in this layer relative to the main IMC layer. The EPMA data from sample 2 are also plotted in Fig. 11 with an adjusted "ternary" composition. The lower Cu concentration in this layer is a result of the reduced Cu content of the stainless steel substrate, which is now adjacent to the IMC layer after depletion of the Cu plating. Thus, both IMC layers in sample 2 are likely the same phase but with only slightly differing compositions. In summary, when the Cu plating layer is depleted, a Cu-rich IMC is no longer stable and the IMC develops a different, lower Cu, composition between the main IMC layer and the low-Cu stainless steel. A separate high-temperature/short time study would be required, involving samples of Cu-plated stainless steel soldered with In–Sn alloy, to definitively analyze the changes in layer compositions accompanying the depletion of the plated Cu layer. In addition, such a study could shed light on the possible changes in *kinetics* that may occur when the Cu source for Cu–In–Sn IMC layer growth becomes depleted.

Note that the anomalously large IMC crystal (Fig. 6a and b), as well as the IMC particles within the solder field (Fig. 6c), had the same composition as the adjacent IMC layer. The measured composition of these phases was 21.6 ± 0.2 wt% Cu, 51.3 ± 0.3 wt% In, 26.6 ± 0.2 wt% Sn (in at.%, 33.6Cu–44.2In–22.2Sn), corresponding to the $Cu_2In_3Sn$ phase. The Cu concentration appears to be too low and the indium content too high to correspond to equilibrium $\eta$ phase. The morphology of the particles suggests that they formed during solidification. However, with such long solid-state diffusion times it is possible that the phase solidified as $\eta$ and later transformed to $Cu_2In_3Sn$ during long-term storage due to the diffusion of Cu within the solder. It is possible that this transformation could even occur during cooling from the soldering temperature. Solidification as $Cu_2In_3Sn$ would agree with the proposed solidification sequences of Velikanova et al., partially based on the work by Liu et al. [8, 12]. In contrast, solidification as $\eta$ phase would be in agreement with the recent experimental work by Lin and coworkers [13]. In that work, the liquidus projection in the Cu–In–Sn system was determined and no evidence was found for ternary $Cu_2In_3Sn$ in equilibrium with the liquid. These contradictory interpretations highlight the need for further work to confirm the solidification sequence and solid-state reactions, especially at low temperatures, in the Cu-poor region of the ternary phase diagram.

Finally, it should be emphasized that the stainless steel *does* contain approximately 3 at.% Cu. This Cu concentration may still support Cu–In–Sn IMC layer growth, albeit to a limited degree. Figure 12 shows close-up views of the EPMA traces from sample 2 (no residual Cu plating layer) at the stainless steel/IMC interface. For clarity, the positions of the stainless steel/IMC interfaces in the traces are displaced slightly from each other. The slight decrease in Cu concentration immediately adjacent to the IMC layer suggests that Cu is being drawn directly from the stainless steel and into the growing IMC layer.

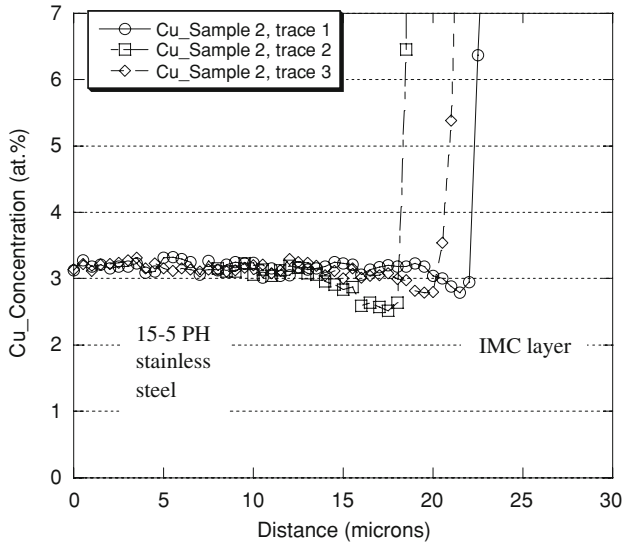



**Fig. 12** Close-up view of the Cu concentration near the stainless steel/IMC interface for the three traces from sample 2. A slight decrease in Cu concentration is observed within the stainless steel adjacent to the interface. The interfaces from the three traces are displaced relative to each other for clarity

## Conclusions

A study was performed to examine the long-term aging effects in In–Sn solder plugs attached to Cu-plated 15-5 PH stainless steel housings. The major findings of this investigation are summarized as follows:

1. The average In–Sn alloy melting onset temperature (solidus) found in this study was 116 °C (241 °F). This value is lower than the values of 118–120 °C of virgin solder alloy. The depression of the melting temperature range was caused by the diffusion of Cu into the solder alloy during solder processing and long-term aging.
2. The Cu–In–Sn IMC layer was thin compared to the overall diameter of the thermal switch solder plugs. The thickest IMC observed was 132 μm, which was associated with large IMC crystal growth. The *average* thickness was 34 ± 8 μm (17 μm on each side of the cross-sectioned solder plug).
3. Combining the results of a previous kinetics study and data from the present work, agreement was found between the predicted IMC thicknesses from the previous work and measured IMC thicknesses for the long-term aged units in this study. Nearly complete depletion of the Cu plating layer occurred, which also allowed the incorporation of small amounts of Fe and Ni from the stainless steel substrate into the IMC layer.
4. The primary (thickest) IMC layer was determined to be $Cu_2In_3Sn$. A thinner IMC layer, adjacent to the stainless steel, had a more Cu-rich composition or Cu-lean composition, depending on whether a residual Cu-plating layer still remained on the stainless steel.
5. Small Kirkendall porosity was observed in some areas of the stainless steel/IMC interface. The Kirkendall voids were generally associated with depletion of the Cu plating layer. The voids were not sufficiently numerous to threaten the hermeticity of any of the observed samples.

**Acknowledgements** The authors would like to thank Dr. Mike Dugger for careful review of the manuscript. Sincere thanks also to Alice Kilgo for metallography and to Bonnie McKenzie for SEM analysis. Sandia is a multiprogram laboratory operated by Sandia Corporation, a Lockheed Martin Company, for the US Department of Energy's National Nuclear Security Administration under Contract DE-AC04-94AL85000.

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